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10/542,903	07/20/2005	Jason R Hector	GB 030043	1786

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EXAMINER	
RAINEY, ROBERT R	
ART UNIT	PAPER NUMBER
2629	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/542,903	HECTOR ET AL.	
	Examiner	Art Unit	
	ROBERT R. RAINEY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *32-36* is/are allowed.

6)☒ Claim(s) *1-6,10,17,18,20,21 and 23-31* is/are rejected.

7)☒ Claim(s) *7-9,11-16,19 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 4/30/2008 regarding the requirement for an election of species have been fully considered but they are not persuasive. The argument that the requirement for an election of species was improper because of a lack of burden on the office is not persuasive because the instant application is a national stage application of a PCT application for which lack of unity rules apply and burden is not part of the consideration for lack of unity. The simple statement without supporting arguments that the invention forms a single inventive concept is not an adequate traversal.

2. Applicant's arguments filed 12/06/2007 regarding the rejections of claims 1 and 27 under 35 U.S.C. 112 are persuasive and the rejections are withdrawn.

3. Applicant's arguments filed 12/06/2007 regarding the objection to claim 17 are persuasive and the objection is withdrawn.

4. Applicant's arguments filed 12/06/2007 with respect to the 35 U.S.C. 103 rejections of claims 1-36 have been considered but are moot in view of the new ground(s) of rejection.

Election/Restrictions

5. The election requirement between species 1-6, as set forth in the Office action mailed on 3/19/2008, has been reconsidered in view of the allowability of claim 32, the limitations of which constitute a special technical feature common to all species, which

thus have unity of invention. All withdrawn claims are therefore reinstated and are examined on the merits.

Claim Objections

6. Claim 4 objected to because of the following informalities: the claim does not end with a period. Appropriate correction is required.

Drawings

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "A.sub.2" and "A.sub.3" have both been used to designate the transistor that turns on the drive transistor and the one that shorts the node between C.sub.1 and C.sub.2 to the source terminal of the drive transistor. It appears for example that Fig. 11 has the usage reversed from that of Fig. 3, 7, 11, 13 and 17. Note that this change in usage is also reflected in claims 19 and 20. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective

action in the next Office action. The objection to the drawings will not be held in abeyance.

8. The drawings are objected to because: Fig. 11 is missing a connection symbol at the point where the line between the OLED and T.sub.D and the line between A.sub.3 and A.sub.4 cross (see [0107] of the instant application). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 1-6, 10, 17, 18, 20, 21, and 23-30** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2005/0156829 to *Choi et al.* ("*Choi*") in view of U.S. Patent Application Publication No. 2003/0052843 to *Yamazaki et al*. ("*Yamazaki*").

As to **claim 1**, *Choi* discloses an active matrix device comprising an array of display pixels (see for example Fig. 1 and [0006]), each pixel comprising: a current driven light emitting display element (2) (see for example Fig. 2 "OELD" and [0041]; note that an "OLED" is a type of "OELD"); a PMOS or NMOS drive transistor (T.sub.D) (see for example Fig. 2 "M3" and [0051] and [0060]) for driving a current through the display element; first and second capacitors (C.sub.1, C.sub.2) (see for example Fig. 2 with C1 corresponding to C.sub.1 and C2 corresponding to C.sub.2) connected in series between the gate and source (see for example Fig. 2 and [0041]-[0043]) or drain of the drive transistor, a data input to the pixel being provided to the junction between the first and second capacitors (C.sub.1, C.sub.2) (see for example Fig. 2 and [0041]-[0043]) thereby to charge the second capacitor (C.sub.2) to a voltage derived from the pixel data voltage (see for example [0049] and Fig. 2 and 3), and a voltage derived from the

drive transistor threshold voltage being stored on the first capacitor (C.sub.1) (note that [0008]-[0009] and Equation 1 describe the relationship between the transistor threshold voltage, V.sub.TH, and the current flowing through the EL device and [0041]-[0049] and Fig. 4 describe how a voltage Vc stored on C1 depends on the current through the EL device and thus on V.sub.TH).

Choi does not expressly disclose that the drive transistor is an amorphous silicon transistor.

Yamazaki discloses and OLED display (see for example [0002]) and in particular such a display utilizing amorphous silicon transistors as one of several interchangeable types (see for example [0025]).

Choi and *Yamazaki* are analogous art because they are from the same field of endeavor, which is OELD displays.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to utilize amorphous silicon transistors as taught by *Yamazaki* as the drive transistors in the device of *Choi*. The suggestion/motivation would have been to utilize an art recognized alternative.

As to **claim 2**, in addition to the rejection of claim 1 over *Choi* and *Yamazaki*, *Choi* further discloses that each pixel further comprises an input first transistor (A.sub.1) connected between an input data line (32) and the junction between the first and second capacitors (C.sub.1, C.sub.2) (see for example Fig. 2 "M1").

As to **claim 3**, in addition to the rejection of claim 1 over *Choi* and *Yamazaki*, *Choi* further discloses a p-type drive transistor with the source of the drive transistor connected to a power supply line (see for example Fig. 2 "M3") and that n-type transistors could be substituted for the p-type transistors (see for example [0051] and [0060]).

Examiner takes official notice that one of ordinary skill in the art at the time of the invention would have known of the differences between p-type and n-type transistors and that in making such a substitution one would connect the drain of the n-type transistor to the power supply. This is evidenced for example by Choi's statement at [0060].

As to **claim 4**, in addition to the rejection of claim 1 over *Choi* and *Yamazaki*, *Choi* further discloses that each pixel further comprises a second transistor (A.sub.2) connected between the gate and drain of the drive transistor (see for example Fig. 2 "M2").

As to **claim 5**, in addition to the rejection of claim 4 over *Choi* and *Yamazaki*, *Choi* further discloses that the second transistor (A.sub.2) is controlled by a first gate control line which is shared between a row of pixels (see for example Fig. 2 line 130; note that this is a gate control line since it controls the gate of the transistor).

As to **claim 6**, in addition to the rejection of claim 1 over *Choi* and *Yamazaki*, *Choi* further discloses that the first and second capacitors (C.sub.1, C.sub.2) are connected in series between the gate and source of the drive transistor (T.sub.D) (see for example Fig. 2 and [0041]-[0043]).

As to **claim 10**, in addition to the rejection of claim 1 over *Choi* and *Yamazaki*, *Choi* further discloses a p-type drive transistor and the first and second capacitors (C.sub.1, C.sub.2) connected in series between the gate and source of the drive transistor (T.sub.D) (see for example Fig. 2 and [0041]-[0043]) and that n-type transistors could be substituted for the p-type transistors (see for example [0051] and [0060]).

Examiner takes official notice that one of ordinary skill in the art at the time of the invention would have known of the differences between p-type and n-type transistors and that in making such a substitution one would connect the drain of the n-type transistor to the power supply. This is evidenced for example by Choi's statement at [0060].

As to **claim 17**, in addition to the rejection of claim 1 over *Choi* and *Yamazaki*, *Choi* further discloses that the capacitor arrangement (C.sub.1, C.sub.2) is connected between the gate and source of the drive transistor

(T.sub.D) (see for example Fig. 2) and that n-type transistors could be substituted for the p-type transistors (see for example [0051] and [0060]).

Examiner takes official notice that one of ordinary skill in the art at the time of the invention would have known of the differences between p-type and n-type transistors and the different connections required to allow the invention to function with n-type including that the source of the drive transistor is connected to a ground line. This is evidenced for example by Choi's statement at [0060].

As to **claim 18**, in addition to the rejection of claim 17 over *Choi* and *Yamazaki*, *Choi* further discloses

Examiner takes official notice that load control in both the high-side as in Choi and the low-side as in the claimed invention and the availability of the one as an alternative to the other were known to those skilled in the art at the time of the invention thus making it obvious to substitute a configuration wherein the drain of the drive transistor (T.sub.D) is connected to one terminal of the display element (2) the other terminal of the display element being connected to a power supply line for the configuration of *Choi*. Examiner personally designed both high-side and low-side transistor amplifiers to control LED's before the time of the invention.

As to **claim 20**, in addition to the rejection of claim 17 over *Choi* and *Yamazaki*, *Choi* further discloses that each pixel further comprises a third

transistor (A.sub.3) connected between the gate and drain of the drive transistor (see for example Fig. 2 "M2").

As to **claim 21**, in addition to the rejection of claim 20 over *Choi* and *Yamazaki*, *Choi* further discloses that the third transistor (A.sub.3) is controlled by a first gate control line which is shared between a row of pixels (see for example Fig. 2 line 130; note that this is a gate control line since it controls the gate of the transistor).

As to **claim 25:24:23**, in addition to the rejection of claim 1 over *Choi* and *Yamazaki*:

Examiner takes official notice that the use of diode-connected transistors in power supply lines was known to those skilled in the art at the time of the invention to be used for several purposes such as to provide a temperature dependent and thus temperature compensating voltage drop or to protect against reverse bias currents or to provide a small change in voltage. It would have been obvious to add a second drive transistor provided between a power supply line (26) and the first drive transistor (T.sub.D) wherein the gate and drain of the second drive transistor are connected together, i.e. diode-connected, for any of the known reasons.

As to **claim 26:23**, in addition to the rejection of claim 1 over *Choi* and *Yamazaki*:

Examiner takes official notice that replacing a single transistor with two in series in order either to reduce leakage current or reduce the effective capacitive load of the transistors in their off state was known to those skilled in the art at the time of the invention. It would have been obvious to add a second drive transistor provided between the first drive transistor (T.sub.D) and the display element (2) for either of these known reasons.

As a separately valid argument for obviousness: It would have been obvious to one having ordinary skill in the art at the time the invention was made to add a second drive transistor provided between the first drive transistor (T.sub.D) and the display element (2), since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co , 193 USPQ 8.

As to **claim 27**, in addition to the rejection of claim 26 over *Choi* and *Yamazaki*:

Examiner takes official notice that adding a transistor connected between the gate and drain of another transistor was well known to those skilled in the art at the time of the invention. It was known to use such a configuration to provide buffering or logic inversion or a timing offset or a drive voltage level conversion. This type of configuration is sometimes referred to as a Darlington-Pair-type.

It would have been obvious to add a transistor (A.sub.5) connected between the gate and drain of the second drive transistor (T.sub.S) for any of the known reasons.

As to **claim 28**, in addition to the rejection of claim 26 over *Choi* and *Yamazaki*:

Examiner takes official notice that adding a transistor connected between the gate of a transistor and a ground potential line was well known to those skilled in the art at the time of the invention. It was known to use such a configuration to provide buffering or logic inversion or a timing offset or a drive voltage level conversion. Examiner personally implemented each of these types of transistor circuits before the time of the invention.

It would have been obvious to add a transistor (A.sub.5) connected between the gate and drain of the second drive transistor (T.sub.S) for any of the known reasons.

As to **claim 29**, in addition to the rejection of claim 1 over *Choi* and *Yamazaki*, *Choi* further discloses a p-type drive transistor with the source of the drive transistor connected to a power supply line (see for example Fig. 2 "M3") and that n-type transistors could be substituted for the p-type transistors (see for example [0051] and [0060]).

Examiner takes official notice that one of ordinary skill in the art at the time of the invention would have known of the differences between p-type and n-type transistors and that in making such a substitution one would connect the drain of the n-type transistor to the power supply. This is evidenced for example by Choi's statement at [0060].

As to **claim 30**, in addition to the rejection of claim 1 over *Choi* and *Yamazaki*, *Choi* further discloses that the display element comprises an electroluminescent (EL) display element (see for example [0002]).

11. **Claim 31** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2005/0156829 to *Choi et al.* ("*Choi*") in view of U.S. Patent Application Publication No. 2003/0052843 to *Yamazaki et al*. ("*Yamazaki*") and further in view of U.S. Patent Application Publication No. 2002/0030647 to *Hack et al*. ("*Hack*").

As to **claim 31**, in addition to the rejection of claim 1 over *Choi* and *Yamazaki*,

Choi and *Yamazaki* does not expressly disclose that the electroluminescent (EL) display element comprises an electrophosphorescent organic electroluminescent display element.

Hack discloses an active matrix OLED display and in particular that the electroluminescent (EL) display element comprises an electrophosphorescent organic electroluminescent display element (see for example [0013]).

Choi, *Yamazaki* and *Hack* are analogous art because they are from the same field of endeavor, which is OELD displays.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to use an electrophosphorescent organic electroluminescent display element as taught by *Hack* to replace the fluorescent organic EL material in the device of *Choi* and *Yamazaki*. The suggestion/motivation would have been to provide advantages such as to improve energy efficiency (see for example *Hack* [0013]).

Allowable Subject Matter

12. **Claims 7-9, 11-16, 19, and 22** objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding **claims 14-16 and 22**, the prior art of record does not teach limitations of claim 1 in conjunction with the limitation of a fourth transistor connected between the drive transistor source and a ground potential line as recited in claim 14. Claim 22 is the analog of claim 14 with the logic reversed

such that the fourth charging transistor (A.sub.4) is connected between a power supply line (50) and the drain of the drive transistor.

Regarding **claims 7-9, 11-13 and 19**, the prior art of record does not teach limitations of claim 1 in conjunction with the limitation of a transistor that connects the node between the capacitors, i.e. input node, to the source of the drive transistor as is claimed in claims 7, 11, and 19.

13. **Claims 32-36** allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not teach the limitations of claim 32, and in particular does not teach: driving a current through the drive transistor (T.sub.D) to ground, and charging a first capacitor (C.sub.1) to the resulting gate-source voltage; discharging the first capacitor (C.sub.1) until the drive transistor turns off, the first capacitor thereby storing a threshold voltage; charging a second capacitor (C.sub.2), in series with the first capacitor between the gate and source or drain of the drive transistor, to a data voltage. By contrast: Choi teaches charging the first capacitor to the difference between an applied voltage and the gate voltage of the drive transistor when the drive transistor is diode connected.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent Application Publication No. 2005/0104814 to Choi et al. is similar to the Choi reference used in the rejections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINEY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629